REMARKS

Applicant is in receipt of the Office Action mailed May 27, 2005. Claims 1-5 were pending in the application. Claims 1-5 have been amended. Claim 6 has been added. Accordingly, claims 1-6 are now pending in the application.

35 U.S.C. § 103 Rejection

Claims 1-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Embree (U.S. Patent 6,104,222) in view of Adams (U.S. Patent 5,638,010).

Applicant notes that to establish a prima facie obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Applicant respectfully submits that even if the cited references were to be combined, the combination would not produce Applicant's invention as claimed in claims 1-5.

Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest, "an analog preconditioner, wherein the analog preconditioner is operable to receive an input clock signal and a master clock signal, wherein the analog preconditioner is configured to output a modified clock signal that is synchronized to the master clock signal", "the analog preconditioner is configured to noise shape phase noise of the synchronization to higher frequencies", and "the digital phase locked loop is also operable to receive the master clock signal, wherein the digital phase locked loop is configured to output an output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal" as recited by amended claim 1. (Emphasis added)

The Examiner contends that these features are taught in Fig. 2, element 150 and column 3, line 57 – column 4, line 25 of Embree. Applicant respectfully disagrees.

Embree fails to teach or suggest that the combination of elements 110, 120, 125, 130 and 140 receive "a master clock signal" as recited in claim 1 and that the PLL circuit 150 "also receives a master clock signal" as recited in claim 1. Embree also fails to teach or suggest that the output of VCO 130 (or the output element 140) and the output of PLL circuit 150 both are "synchronized to the master clock signal" as recited in claim 1.

The Examiner further contends, "It is noted that in Embree, the reset signal (Figure 2), which synchronizes all the circuit components in system 100, teaches "the master clock", which is received by both "preconditioner" and the phase locked loop." Applicant respectfully disagrees. Embree uses a synchronous reset signal to synchronize the down-dividers (110, 140, 156, 160, and 170) to achieve fast lock times. (Emphasis added) (see Embree, column 4, line 61 – column 5, line 7 and column 5, line 63 – column 6, line 23) Applicant notes that Embree teaches a synchronous reset signal, not a "master clock signal". Also, Applicant submits that Embree fails to teach "the analog preconditioner is configured to" synchronize "an input clock signal" to a "master clock signal" to "noise shape phase noise of the synchronization to higher frequencies". (Emphasis added)

In accordance, claim 1 is believed to patentably distinguish over Embree and Adams, whether alone or combined. Claims 2-5 depend on claim 1 and are therefore believed to patentably distinguish over Embree and Adams, whether alone or combined, for at least the reasons given above.

Additionally, Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest, "the analog preconditioner comprises...a latch including an input coupled to the output of the VCO, an input which is operable to receive the master clock signal, and also including an output which is operable to generate the modified clock signal, wherein the latch is configured to synchronize the modified clock signal to the master clock signal, wherein the output of the latch is coupled to the second input of the phase detector to provide the modified clock signal to the phase detector" as recited by claim 5.

The Examiner contends that these features are taught in Fig. 2, element 140 of Embree. Applicant submits that Embree fails to teach or suggest element 140 having "an input which receives the master clock signal" as recited by claim 5, and Embree further fails to teach or suggest that element 140 "synchronizes" the output of the VCO 130 " to the master clock signal" as recited by claim 5. Also, as shown in Figure 2 of Embree, Embree fails to teach or suggest that "the output" of element 140 "is coupled to" an "input of the phase detector" 120 as recited by claim 5.

The Examiner also contends that the above-highlighted features of claim 5 are taught by elements 70, 85, 87, and 88 on Figure 3 of Abrams. Applicant respectfully submits that Figure 3 of Abrams fails to teach or suggest "an analog preconditioner" including the features highlighted above and coupled to a DPLL. In fact, Abrams teaches away from using an "analog preconditioner" in column 2, lines 14-19, "It is preferable to use a digital PLL to provide a single digital integrated circuit which accommodates a number of input sample rates but which eliminates the requirement of an analog PLL and allows a user to provide only an asynchronous master clock instead of a master clock phase-locked to the input rate". (Emphasis added) Accordingly, claim 5 is believed to patentably distinguish over Embree and Adams, whether alone or combined.

Furthermore, Applicant respectfully requests examination of new claim 6. Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest, "the analog preconditioner is configured to noise shape phase noise of the VCO to higher frequencies" as recited by claim 6. Accordingly, claim 6 is believed to patentably distinguish over Embree and Adams, whether alone or combined.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant submits the application is now in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-47800/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☒ Request for Continued Examination

Respectfully submitted,

Jeffrey C. Hood
Reg. No. 35,198
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800
Date: 9/27/2005 JCH/MJL